What is claimed is:

[Claim 1] 1. A heterobipolar transistor (HBT) comprising:

a substrate including at least a subcollector;

a buried refractory metal silicide layer located on the subcollector; and

a shallow trench isolation region located on a surface of said buried refractory metal silicide layer.

[Claim 2] 2. The HBT of Claim 1 wherein said substrate comprising a semiconductor substrate selected from the group consisting of Si, SiGe, SiC, SiGeC, GaAs, InAs, InP, silicon-on-insulators, silicon germanium-on-insulators, and other III/V or II/VI compound semiconductors.

[Claim 3] 3. The HBT of Claim 2 wherein said semiconductor substrate is Si-containing.

[Claim 4] 4. The HBT of Claim 1 wherein said subcollector is doped with C.

[Claim 5] 5. The HBT of Claim 1 wherein said shallow trench isolation region and said buried refractory metal silicide layer are located in an opening that comprises nitride or oxynitride spacers.

[Claim 6] 6. The HBT of Claim 1 wherein said refractory metal silicide layer comprises a silicide of Ti, Co, W, Ta, Ni or alloys thereof.

[Claim 7] 7. The HBT of Claim 6 wherein said refractory metal silicide layer comprises a silicide of Co, Ta or W.

[Claim 8] 8. The HBT of Claim 7 wherein said refractory metal silicide layer comprises a silicide of W.

[Claim 9] 9. The HBT of Claim 1 wherein said shallow trench isolation region comprises a trench dielectric material.

[Claim 10] 10. The HBT of Claim 1 wherein said refractory metal silicide layer extends beyond the edges of the shallow trench isolation region such that a portion of said refractory metal silicide layer is present in an undercut region.

[Claim 11] 11. The HBT of Claim 10 wherein said refractory metal silicide layer comprises a silicide of Ti, Co, W, Ta, Ni or alloys thereof.

[Claim 12] 12. The HBT of Claim 11 wherein said refractory metal silicide layer comprises a silicide of Co, Ta or W.

[Claim 13] 13. The HBT of Claim 12 wherein said refractory metal silicide layer comprises a silicide of W.

[Claim 14] 14. The HBT of Claim 1 further comprising a SiGe base and a polySi emitter located on said substrate including said subcollector.

[Claim 15] 15. A method of fabricating a heterobipolar transistor (HBT) comprising the steps of:

forming at least one shallow trench isolation region containing a first trench dielectric material in a substrate including a subcollector;

removing said first trench dielectric material from said at least one shallow trench isolation region to form an opening that exposes a portion of said substrate including said subcollector;
forming a refractory metal silicide layer in a portion of said opening on said exposed portion of the substrate, said refractory metal silicide layer not extending above said opening; and

forming a second trench dielectric on said refractory metal silicide layer in said opening, said second trench dielectric not extending above said opening.

[Claim 16] 16. The method of Claim 15 wherein said at least one shallow trench isolation is formed by lithography, etching and trench fill.

[Claim 17] 17. The method of Claim 16 further comprising at least one of a densification or planarization process.

[Claim 18] 18. The method of Claim 16 further comprising implanting C into said subcollector prior to trench fill.

[Claim 19] 19. The method of Claim 15 wherein said removing of said first trench dielectric material comprises a selective etching process.

[Claim 20] 20. The method of Claim 15 further comprising forming nitride or oxynitride spacers between the steps of removing said first trench dielectric material and forming said refractory metal silicide.

[Claim 21] 21. The method of Claim 15 wherein said forming said refractory metal silicide layer comprising depositing a refractory metal layer and annealing.

[Claim 22] 22. The method of Claim 21 further comprising forming a silicon layer prior to depositing.

[Claim 23] 23. The method of Claim 21 wherein said depositing comprises a selective deposition process.

[Claim 24] 24. The method of Claim 21 wherein said depositing comprising a non-selective deposition process.

[Claim 25] 25. The method of Claim 21 wherein said annealing comprises a first annealing step and removing unreacted refractory metal.

[Claim 26] 26. The method of Claim 25 wherein said first annealing step is conducted at a temperature from about 400°C to about 700°C.

[Claim 27] 27. The method of Claim 21 further comprising a second annealing step performed after said removing of unreacted refractory metal.

[Claim 28] 28. The method of Claim 27 wherein said second annealing step is performed at a temperature from about 700°C to about 1100°C.

[Claim 29] 29. The method of Claim 15 wherein said removing said first trench dielectric material comprises forming a patterned photoresist that protects a portion of said at least one shallow trench isolation region.

[Claim 30] 30. The method of Claim 29 further comprising forming an undercut region using a lateral etching process.